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Al-Rich AlGaN Transistors with Regrown p-AlGaN Gate Layers and Ohmic Contacts

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Epitaxial regrowth processes are presented for achieving Al-rich aluminum gallium nitride (AlGaN) high electron mobility transistor (HEMTs) with p-type gates with large, positive threshold voltage for enhancement mode operation and low resistance Ohmic contacts. Utilizing a deep gate recess etch into the channel and an epitaxial regrown p-AlGaN gate structure, an $Al_{0.85}Ga_{0.15}N$ barrier/$Al_{0.50}Ga_{0.50}N$ channel HEMT with a large positive threshold voltage ($V_{TH} = +3.5$ V) and negligible gate leakage is demonstrated. Epitaxial regrowth of AlGaN avoids the use of gate insulators which can suffer from charge trapping effects observed in typical dielectric layers deposited on AlGaN. Low resistance Ohmic contacts (minimum specific contact resistance $= 4 \times 10^{-6}$ Ω cm^2, average $= 1.8 \times 10^{-4}$ Ω cm^2) are demonstrated in an $Al_{0.85}Ga_{0.15}N$ barrier/$Al_{0.68}Ga_{0.32}N$ channel HEMT by employing epitaxial regrowth of a heavily doped, n-type, reverse compositionally graded epitaxial structure. The combination of low-leakage, large positive threshold p-gates and low resistance Ohmic contacts by the described regrowth processes provide a pathway to realizing high-current, enhancement-mode, Al-rich AlGaN-based ultra-wide bandgap transistors.

1. Introduction

Ultra-wide bandgap (UWBG) semiconductors are in a growing field of study focusing on materials with bandgaps beyond that of gallium nitride (GaN). These materials,[1] including aluminum gallium nitride (AlGaN), gallium oxide (Ga_2O_3), diamond, and cubic boron nitride (cBN), have qualities that make them suitable for extreme operating conditions beyond that of conventional materials. Their large bandgaps support a higher theoretical breakdown field, which contributes to a heightened lateral figure of merit.[2] These same bandgaps suppress thermal effects that normally limit silicon-based electronics at higher ambient conditions (>250 °C), allowing for operation in extreme temperatures.[3] Additionally, the stronger atomic bonding of these materials results in improved radiation tolerance,[2,4] making them more amenable to satellite applications. Among the UWBG technologies, Al-rich AlGaN high electron mobility transistors (HEMTs) have AlN native substrates with a better thermal conductivity than Ga_2O_3 and more mature fabrication techniques compared to diamond and cBN. The advantages of Al-rich AlGaN have the potential to enable the next generation of power transistors, but improvements in the technology are needed.

Two primary requirements of power transistors are enhancement-mode threshold voltages (V_{TH}) with positive turn-on voltages for fail-safe operation and low on-resistance (R_{ON}) for high efficiency and output power. For the first requirement, enhancement-mode AlGaN HEMTs have been previously realized through methods analogous to those used for GaN channel HEMTs,[5–7] such as the inclusion of a p-AlGaN layer underneath the gate electrode[8] or treating the HEMT barrier in the gate area with a combination of recess etching and F^- ion implantation.[9] These techniques rely on spatial control of 2D electron gas (2DEG) carrier populations, ideally producing a structure with minimal carriers in the gate area and maximum carriers in the access and Ohmic regions. To operate at high drain currents, transistors with increasingly positive threshold voltage (>1 V) must maintain minimal forward gate leakage current at gate biases well above V_{TH}. Prior Al-rich AlGaN HEMT publications lack simultaneously high positive V_{TH} and large voltage swings.

For the second requirement, resistive source and drain electrodes degrade R_{ON} in Al-rich AlGaN devices because of the large Schottky barrier that forms at metal-semiconductor interfaces due to the low electron affinity of the AlGaN.[10] Several prior reports have examined strategies to realize Ohmic contacts to Al-rich AlGaN including planar,[11–14] Si-implanted,[15,16] compositionally reverse-graded contact layers,[10,17,18] recess etching and compositionally reverse-graded regrowth,[19] pulse sputtering deposition doped contacts,[20] and polarization-doped contacts.[21]

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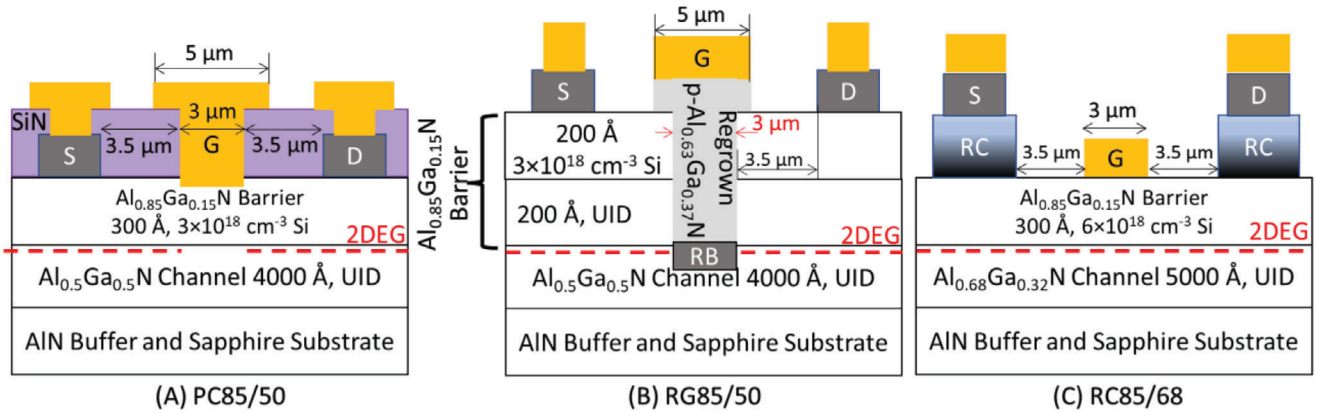

Figure 1. Transistor epitaxial architectures and layout indicating locations of the source (S), gate (G), drain (D), regrown barrier (RB), regrown contact (RC), and 2D electron gas (2DEG).

This report describes a series of experiments to realize the above requirements. First, improved Ohmic contacts to a transistor with an $Al_{0.85}Ga_{0.15}N$ barrier were realized by reducing the $Al_xGa_{1-x}N$ channel composition from x = 70% to 50% and growing the channel sufficiently thick to induce partial relaxation of the epilayer. Although improved contacts were achieved, the gate, a Schottky contact to the barrier, exhibited forward conduction that limited the practical V_{TH} range to <1 V. To overcome this limitation, the $Al_{0.85}Ga_{0.15}N$ barrier/$Al_{0.5}Ga_{0.5}N$ channel HEMT was constructed with a deep recess etch into the channel followed by a regrown barrier and p-$Al_{0.65}Ga_{0.35}N$ epi structure to serve as the gate. These devices exhibited a large V_{TH} = +3.5 V and low forward gate current, but the inclusion of an undoped barrier layer to minimize Schottky gate forward conduction likely degraded Ohmic contacts and hence the drain current. The last experiment developed low-resistance Ohmic contacts to an $Al_{0.85}Ga_{0.15}N$ barrier/$Al_{0.68}Ga_{0.32}N$ channel using an epitaxially regrown, heavily doped n-type and compositionally reverse-graded epi structure. This structure demonstrated significantly lower Ohmic contact resistivity compared to planar metal contacts to $Al_{0.85}Ga_{0.15}N$ barrier/$Al_{0.5}Ga_{0.5}N$ HEMTs.

Throughout this work, gate insulators were not employed as they can promote charge trapping effects due to non-epitaxial and/or non-stoichiometric methods of depositing typical dielectric layers on AlGaN. Rather, metal-semiconductor junctions were used at all gates. The methods in this report establish the framework to realize Al-rich AlGaN power transistors. By combining the etched and regrown gates with the regrown graded contacts developed in the present work, a new generation of AlGaN power transistors will be realized.

2. Experimental Section

Epitaxial structures were grown using metal-organic chemical vapor deposition (MOCVD) on previously prepared 2 inch diameter AlN/sapphire templates using a Taiyo Nippon Sanso SR4000-HT reactor. Three distinct epitaxial HEMT structures were used for this report, graphically represented in **Figure 1**. First, a planar source/drain (S/D) contact structure named **PC85/50**, had a 4000 Å $Al_{0.5}Ga_{0.5}N$ channel and a 300 Å $Al_{0.85}Ga_{0.15}N$ barrier with 3×10^{18} cm^{-3} Si doping. Next, a recessed etched and regrown gate structure, named **RG85/50**, had a 4000 Å $Al_{0.50}Ga_{0.50}N$ channel, a barrier layer consisting of a 200 Å $Al_{0.85}Ga_{0.15}N$ unintentionally doped (UID) layer plus a 200 Å $Al_{0.85}Ga_{0.15}N$ 3×10^{18} cm^{-3} Si doped layer; the gate area was etched to a minimum depth of 400 Å and a subsequent regrowth added 100 Å $Al_{0.85}Ga_{0.15}N$ barrier and a 1000 Å $Al_{0.63}Ga_{0.37}N$ 9×10^{19} cm^{-3} Mg doped p-type layer. Last, a regrown S/D contact structure named **RC85/68** had a 5000 Å $Al_{0.68}Ga_{0.32}N$ channel, a 300 Å $Al_{0.85}Ga_{0.15}N$ barrier with 6×10^{18} cm^{-3} Si doping, and regrown, compositionally reverse-graded (Al grading from 85% to 14%) n++ (Si) contact layer. During regrowth, a mask was used so that the contact layer was regrown only in the S/D areas of the devices.

Throughout wafer fabrication, standard contact lithography was used for all patterning and electron-beam deposition was used for all metallization steps, unless otherwise noted. Prior to each metal deposition, the wafer was cleaned with oxygen plasma followed by hydrochloric acid. All source and drain metal contacts were 250 Å Ti/1000 Å Al/150 Å Ni/500 Å Au and all gate metal contacts were 200 Å Ni/4500 Å Au.

1) **PC85/50**: Ti/Al/Ni/Au Ohmic contacts were deposited and annealed at 1000 °C for 30 s in a ≈1 Torr nitrogen atmosphere. Next, a 1000 Å SiN layer was blanket deposited over the entire wafer, then patterned and reactive ion etched (RIE) in a CF_4/O_2 plasma to define the gate footprint with SiN vias and open electrical access areas to the source and drain. Note that for the gate area the first 370 s of each etches contributed to the removal of the 1000 Å SiN layer over the barrier and the remaining time contributed to the barrier recess etching. The sample was over-etched for a total etch time of 909 s to shift V_{TH} positive by recess etching the barrier while simultaneously implanting fluorine ions to the gate area.[9] Finally, a Ni/Au gate metal was deposited in the gate area and over the S/D contacts.
2) **RG85/50**: The wafer was first lithographically patterned and RIE etched so that the $Al_{0.85}Ga_{0.15}N$ barrier in the gate areas was completely removed. To compare the impact of etch depth, three different etch times were applied to adjacent devices: 1) 2500 s, 400 Å depth, 2) 3125 s, 500 Å depth, and 3) 3750 s, 600 Å depth. The samples were cleaned at 70 °C AZ400K for 2 min and regrown with a 100 Å-thick undoped

Table 1. Extracted average values from devices with 3 μm gate lengths.

Wafer	ρ_c [Ω cm^2]	R_{SH} [Ω sq^{-1}]	L_T [μm]	V_{TH} [V]	$J_{DS,}$max [mA mm^{-1}]	$g_{m,max}$ [mS mm^{-1}]	Ion-off	$J_{DS,off}$ [mA mm^{-1}]
PC85/50	7.4×10^{-4}	2269	6	−2.5	70.65	29.71	1.41×10^5	5.2×10^{-3}
RC85/50	1.8	49560	95	3.5	3.33	1.08	1.41×10^8	2.3×10^{-8}
RC85/68	1.8×10^{-4}	4156	1.9	−6.4	108.20	14.56	2.11×10^9	5.2×10^{-8}

$Al_{0.85}Ga_{0.15}N$ layer followed by a 1000 Å-thick 9×10^{19} cm^{-3} Mg doped $Al_{0.63}Ga_{0.37}N$ layer. The Mg was activated with a 5 min 900 °C anneal, then the wafer was patterned so that the gate areas were covered with resist, and the regrown layers in the access and Ohmic areas were removed with an additional RIE timed etch. Planar Ohmic contacts of Ti/Al/Ni/Au were deposited and annealed at 1000 °C for 30 s. The fabrication was completed by depositing Ni/Au gates in the gate area and over the S/D contacts.

3) **RC85/68**: First, an Ohmic contact regrowth mask was lithographically defined and deposited. Prior to regrowth, the wafer received a 70 °C AZ400K clean for 2 min. Regrowth of the compositionally reverse graded n++ AlGaN contact layer was performed. Next, the excess regrown AlGaN over the mask was selectively removed by photoresist patterning and inductively coupled plasma (ICP) etching, followed by regrowth mask removal with a wet etch. Ti/Al/Ni/Au Ohmic metal was deposited in the regrown areas and annealed at 700 °C for 30 s in a ≈1 Torr nitrogen atmosphere. Last, Ni/Au gate metal was deposited in the gate area and over the S/D contacts.

The resulting transistors were circular with a central drain, an exterior source, and a gate in-between (Figure 1) and had gate lengths (GL) of 1.5, 2, 2.5, and 3 μm. Unless noted otherwise, 3 μm gates were used. The gates were equidistant between the source and drain and the drain-to-source spacing was 10 μm. The gate width, taken at the midline of the gate, was 0.66 mm. Each circular transmission line method (CTLM) test structure had a 200 μm diameter center circular electrode, a gap, and an outer electrode that surrounded the center electrode. There were seven distinct pairs of center/outer electrodes with gap spacings of 5, 10, 15, 20, 25, 30, and 35 μm.

CTLM current–voltage (I/V) sweeps were collected with a Keithley 238 source measure unit and transistor electrical characterization was performed with either a Keysight B1500A or an Agilent 4156C semiconductor parameter analyzer. Specific contact resistance (ρ_c) was extracted from the CTLM sweeps with the methodology described in.[22] The 10, 15, 20, and 25 μm spacings (d) were used for the extraction. First, the total resistance (R_T) was taken from each CTLM I/V sweep using Ohm's Law ($R_T = V/I$). Since the TLM layout was circular, a correction factor was employed: $CF = (L/d)\ \ln(1 + d/L)$, where L was the radius of the inner contact pad. The sheet resistance (R_{SH}) was extracted by taking the slope of R_T/CF plotted as a function of d and multiplying by the contact width (z), which was defined as the perimeter of the central electrode. The x-axis intercept of the R_T/CF plot is equal to twice the transfer length (L_T). Lastly, the specific contact resistance was extracted as the product of the sheet resistance and square of the transfer length (L_T in units of cm): $\rho_c = R_{SH}L_T^2$.

From the transistor I/V sweeps, a MATLAB script extracted V_{TH}, maximum drain current density (J_{DSmax}), maximum transconductance ($g_{m,max}$), on-off drain current ratio (Ion-off), and off-state drain leakage current ($J_{DS,OFF}$). The V_{TH} was defined as the gate bias where the drain current surpasses 100 μA. Extraction results from electrical sweeps for all three samples are summarized in **Table 1**.

3. Results and Discussion

PC85/50 exhibited linear, through-the-origin I/V sweeps (**Figure 2A**). An average specific contact resistance of 7.4×10^{-4} cm^2 was extracted, with some sites as low as 3×10^{-4} Ω cm^2 (R_{SH} = 1647 Ω sq^{-1}, L_T = 4.4 μm). During optimization, where multiple epitaxial structures were fabricated into transistors and compared, the contact resistance was lowest with 1) reduced Al channel composition (tested from 50% to 70% Al), 2) increased Al in the barrier (tested from 60% to 85% Al), and 3) increased channel thickness (tested from 400 to 3600 Å). The combination of a 3600 Å-thick $Al_{0.50}Ga_{0.50}N$ channel and maximized Al contrast, i.e., polarization charge, between the channel and barrier produced the lowest contact resistances but also exhibited increased surface roughness due to partial relaxation of the 3600Å, 50% channel compared to HEMTs with a pseudomorphic grown channel and barrier. The relationship between increased surface roughness and reduced contact resistance implies that the combination of degraded surface morphology and relaxation of compressive strain aid in reducing Ohmic contact resistance.

PC85/50 (electrical sweeps plotted in Figure 2B,C) was a depletion-mode device with V_{TH} = −2.5 V controlled by recess etching of the barrier under the gate. The average $J_{DS,max}$ was 70 mA mm^{-1}, $g_{m,max}$ was 29 mS mm^{-1}, and a relatively low Ion-off ratio for 1×10^5 was observed and attributed to a large off-state leakage current of 5×10^{-3} mA mm^{-1}. A disadvantage of this device was that the Schottky gate forward conduction effectively limited gate biasing to 2 V maximum. Forward gate leakage was observed beyond 1 mA mm^{-1} without the Schottky gate evidencing a turn-on voltage transition to linear conduction. This high gate leakage mechanism could be related to the degradation in surface morphology, and it caused degradation of drain current in devices with increasingly positive V_{TH}. The I_{DS}–V_{DS} sweeps in Figure 2C illustrate both the beneficial effects of low-resistance contacts and the deleterious effects of gate leakage current. The sweeps showed no offset voltage from the origin and J_{DS} exceeded densities of 120 mA mm^{-1} at 4 V gate bias and 5 V drain bias, both desirable attributes. However, I_{GS} reached compliance settings and constrained drain current for gate biases beyond 3 V, limiting voltage swing. To overcome the leakage current setbacks, an

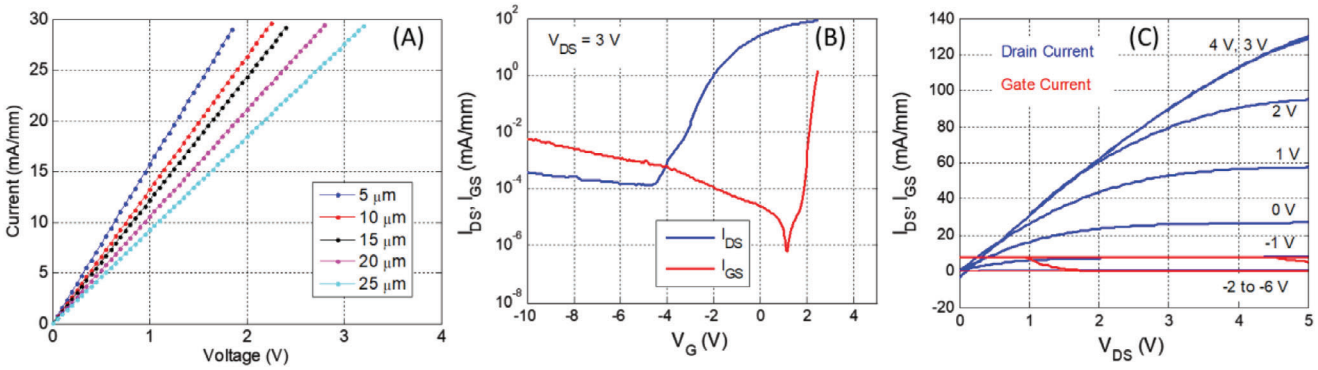

Figure 2. Electrical sweeps of PC85/50 for A) CTLM characterization, B) drain and gate current as a function of gate bias (V_{DS} = 3 V), C) drain and gate current versus drain-to-source bias (V_{GS} = −6–4 V in 1 V increments).

alternate approach to fabricating enhancement-mode gates was investigated next.

The **RG85/50** transistor incorporated two design approaches: 1) planar Ohmic contacts to an $Al_{0.85}Ga_{0.15}N$ barrier/$Al_{0.50}Ga_{0.50}N$ channel HEMT like the PC85/50 transistors and 2) a gate region with recessed and regrown barrier/p-type $Al_{0.63}Ga_{0.37}N$. The latter enabled spatially selective barrier thickness control to realize a device with positive V_{TH} and reduced forward gate leakage. Characteristic plots of the CTLM sweeps, I_{DS}–V_G and I_{DS}–V_{DS} are provided in **Figure 3**. The CTLM measurements revealed an average specific contact resistance of 1.8 Ω cm^2, which is high compared to the PC85/50 sample. We attribute this degraded performance to the inclusion of the 200 Å UID barrier layer, which was intended to reduce gate leakage paths potentially introduced by surface roughening but also likely caused an unintended increase in contact resistance. Because of the increased contact resistance, $J_{DS,max}$ and $g_{m,max}$ had only modest values of 3 mA mm^{-1} and 1 mS mm^{-1}, respectively. An additional resistance contribution from the sidewall of the etched and regrown gate is possible, but because of the large resistance from the contact and sheet resistance contributions (determined by an analysis of the I/V sweeps of the gateless CTLM structures) a gate sidewall resistance cannot be accurately extracted from these devices. Despite this setback, the devices exhibited large positive V_{TH} values of 3.5 V, high Ion-off ratios of 1.4 × 10^8, and low $J_{DS,off}$ of 2.3 × 10^{-8} mA mm^{-1}. The I_{DS}–V_{DS} sweeps in Figure 3C display minimal gate leakage-mediated distortion, in addition to linear through-the-origin sweeps in the transistor linear region. These results show that this alternate gating approach produces low-leakage enhancement-mode transistors and, critically, suppresses the forward-bias gate leakage current up to at least 8 V, thereby enhancing voltage swing.

In future device iterations, the I_{DS} could be increased by changing the design of the barrier to increase electron injection into the 2DEG. More importantly, eliminating the timed access and Ohmic area etch to remove the regrown p-AlGaN may improve $I_{DS,}$ because unless the timed etch depth is exact, the barrier could be over-etched or a p-AlGaN layer over the barrier could remain; either case could increase sheet resistance. Instead, using a mask layer (later removed with a wet etch) for the p-AlGaN regrowth would eliminate the timed access and Ohmic area etch challenges.

Two experimental splits were conducted on the RG85/50 wafer: 1) variable recessing of adjacent devices to depths of 400, 500, and 600 Å, and 2) variable gate lengths of 1.5, 2, 2.5, and 3 μm. In the recessing split (I/V sweeps provided in **Figure** 4A) only a minor etch depth dependence in V_{TH} and gate leakage was observed, which was further confirmed by the extracted mean V_{TH} values collected over five sites across the wafer (results summarized in **Table** 2). For the variable gate length split, the

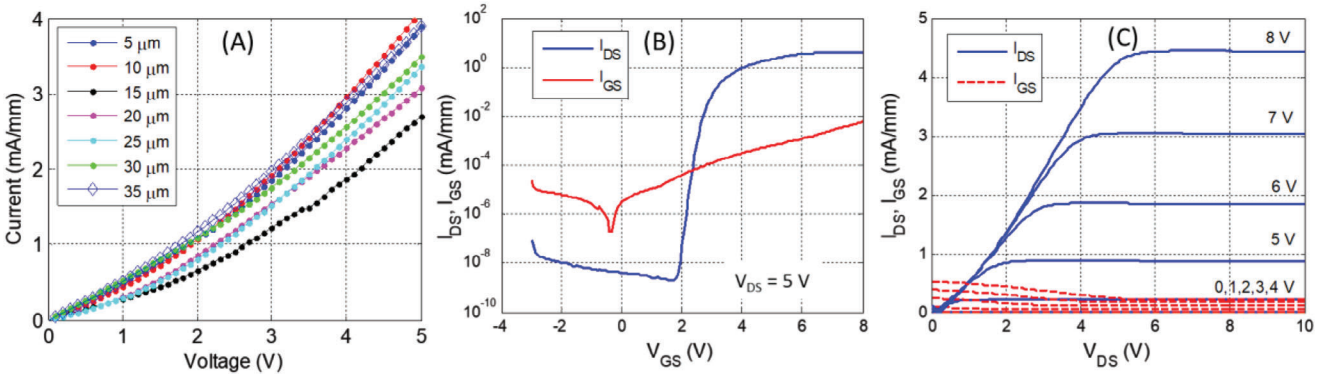

Figure 3. RG85/50 electrical sweeps. A) CTLM, B) drain current versus gate bias (V_{DS} = 5 V), C) drain current versus drain-to-source (V_{GS} = 0 to 8 V in 1 V increments).

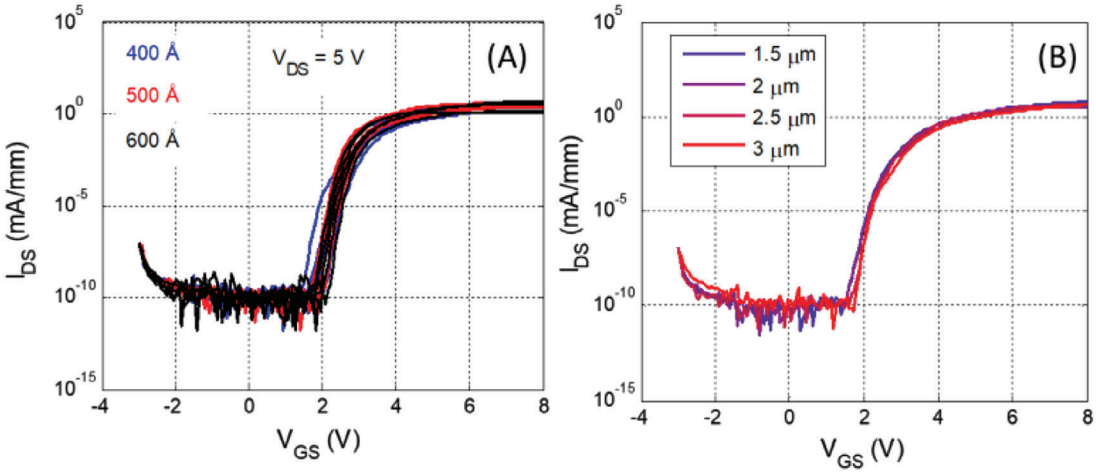

Figure 4. I/V sweeps for A) gate recess depths of 400, 500, and 600 Å and B) variable gate length of 1.5, 2, 2.5, and 3 μm. (V_{DS} = 5 V).

dependence of V_{TH}, $J_{DS,max}$, $g_{m,max}$ and Ion-off is summarized in **Table 3** and a representative set of sweeps is shown in Figure 4B. Douglas et al.[8] had previously observed a V_{TH} dependence with gate length and reported a +1.3 V shift by increasing gate lengths from 1.5 to 3 μm. Comparatively, the switches in the present study did not have strong a V_{TH}-gate length dependence, with only a minor V_{TH} change of +0.22 V from 1.5 to 3 μm. Furthermore, only a minor dependence of $J_{DS,max}$ or $g_{m,max}$ with gate length was observed and the Ion-off ratio remained ≈10^8 for all gate lengths. The minor dependence of gate length and recess depth on transistor electrical characteristics highlight the high level of process stability offered by this approach. However, improvements in Ohmic contacts without surface morphology degradation were still needed. The next sample, RC85/68, addresses that need.

RC85/68 had an average specific contact resistance of 1.8×10^{-4} Ω cm^2, with minimum values of 4×10^{-6} Ω cm^2 (R_{SH} = 4722 Ω sq^{-1}, L_T = 0.28 μm). These contacts relied on degenerate n-type doping and low aluminum composition (Al = 15%) to attain a low contact resistance at the metal-semiconductor interface. These depletion-mode transistors, whose characteristic electrical plots are provided in **Figure 5**, had average V_{TH} = −6.4 V, $J_{DS,max}$ >100 mA mm^{-1} (V_{GS} of 4 V, V_{DS} of 10 V), $J_{DS,off} = 3.4 \times 10^{-8}$ mA mm^{-1}, and Ion-off >2×10^9 This structure has the combination of lower-resistance contacts and low-leakage forward gate characteristics with a turn-on voltage ≈ 2 V (63 μA mm^{-1}). These advantages arise from the spatially defined regrown contact areas, rather than relying on contact formation from the as-grown epi structure, as was the case for PC85/50. The next step for enhancement-mode Al-rich AlGaN power transistor technology is to combine the low-resistance Ohmic contacts of RC85/68 and the low leakage, large positive V_{TH} gates of RG85/50. This ongoing work promises good viability because it incorporates the same proven regrowth mask and fabrication techniques used in the RG85/50 sample described here.

4. Conclusion

Approaches to fabricating Al-rich UWBG AlGaN HEMTs with low resistance Ohmic contacts and p-type gates with large, positive V_{TH} for enhancement mode operation were investigated. Planar Ohmic contacts with minimum $\rho_c = 3 \times 10^{-4}$ Ω cm^2 and average $\rho_c = 7.4 \times 10^{-4}$ Ω cm^2 were realized for the PC85/50 HEMTs with large polarization charge but attendant roughening of the surface morphology due to partial relaxation of the channel layer likely contributed to forward Schottky gate leakage and lower contact resistance. Utilizing a deep gate recess etch into the channel and an epitaxial regrown p-AlGaN gate structure resulted in RG85/50 HEMTs with a large forward threshold voltage (V_{TH} = +3.5 V) and negligible forward gate current, demonstrating the utility of deep trench etch and p-AlGaN gate regrowth for practical enhancement mode transistors. Reverse-graded Ohmic contacts with minimum $\rho_c = 4 \times 10^{-6}$ Ω cm^2 and average $\rho_c = 1.8 \times 10^{-4}$ Ω cm^2 were achieved for RC85/68 HEMTs while maintaining a low forward leakage Schottky contact. The combination of low-leakage, positive threshold p-gates and low resistance Ohmic contacts by the discussed regrowth processes provide a pathway to realizing high-current, enhancement-mode, Al-rich AlGaN-based UWBG transistors.

Table 2. RG85/50: Dependence on gate recess depth from five sites across the wafer. Average values of threshold voltage, max current density, transconductance, and on-off current ratio.

Etch Depth [Å]	V_{TH} [V]	$J_{DS,max}$ [mA mm^{-1}]	$g_{m,max}$ [mS mm^{-1}]	Ion-off
400	3.5	2.9	0.9	1.9×10^8
500	3.3	3.0	1.0	2.1×10^8
600	3.4	3.0	1.0	2.2×10^8

Table 3. RG85/50: Dependence on gate length for average values of threshold voltage, max current density, transconductance, and on-off current ratio from three sites across the wafer.

Gate Length [μm]	V_{TH} [V]	$J_{DS,max}$ [mA mm^{-1}]	$g_{m,max}$ [mS mm^{-1}]	Ion-off
1.5	3.23	4.36	1.53	2.8×10^8
2.0	3.30	3.33	1.23	2.2×10^8
2.5	3.27	3.49	1.16	1.8×10^8
3.0	3.45	3.41	1.12	1.8×10^8

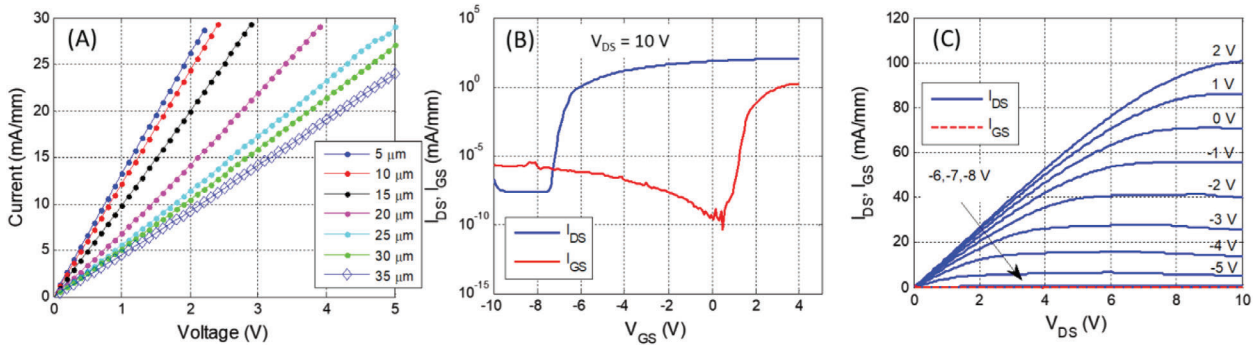

Figure 5. RC85/68 electrical sweeps. A) CTLM, B) drain current versus gate bias (V_{DS} = 10 V), C) drain current versus drain-to-source bias (V_G = 2–−8 in 1 V increments).

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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semiconductors, transistors, ultra-wide bandgaps

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